REMARKS

Applicants appreciate the thorough examination of the present application that is reflected in the Official Action of August 12, 2004. Applicants also appreciate the Examiner's citation of U.S. Patent 4,326,332 to Kenney. In response, Claims 14-19 have been amended to clarify the patentable distinctions over Kenney. Moreover, new Claims 20-24 have been added. Applicants respectfully submit that the pending claims are patentable over Kenney, for the reasons that will now be described.

Claim 14 Is Patentable Over Kenney

Claim 14 stands rejected under 35 USC §102(b) as being anticipated by Kenney. However, Claim 14 has been extensively amended to recite that the integrated circuit substrate includes a planar face, the insulating layer is a planar insulating layer that extends along the planar face of the integrated circuit substrate, and the first conductive layer pattern is a first planar conductive layer pattern that extends along the planar insulating layer opposite the planar face of the integrated circuit substrate. In sharp contrast, in Kenney, the substrate includes a V-groove therein, the insulating layer is a V-shaped insulating layer, and the conductive layer pattern is a V-shaped conductive layer pattern. Accordingly, Claim 14 is not anticipated by Kenney.

Nor would it be obvious to change the V-shaped layers of Kenney to provide planar layers, as recited in Claim 14, because Kenney clearly relates to *"Method of Making a High Density V-MOS Memory Array"*, as recited in the Kenney title. Moreover, Kenney's Background of the Invention, Summary of the Invention and Detailed Description are all directed to V-MOS technology, and improvements thereof. There is no description or suggestion to provide the layers recited in Claim 14 in a planar semiconductor technology. Accordingly, Claim 14 is patentable over Kenney. Claims 15-19 are patentable at least per the patentability of Claim 14 from which they depend.

Finally, Applicants also wish to note that, since the Official Action has not given patentable weight to the preamble limitation "Read Only Memory (ROM) device", this recitation has been eliminated from the preamble of Claim 14, and the preambles of dependent Claims 15-19.

Claims 17 and 18 Are Independently Patentable

Claims 17 and 18 are patentable at least per the patentability of Claim 14 from which they depend. Moreover, Claims 17 and 18 are independently patentable. In particular, Claim 17 recites:

> 17. A device according to Claim 14 further comprising a read only memory programming region in the integrated circuit substrate beneath the planar insulating layer. (Emphasis added.)

Kenney does not describe a ROM device, but, rather, describes a Dynamic Random Access Memory (DRAM) device. As such, Kenney does not describe or suggest a "read only memory programming region in the integrated circuit substrate beneath the planar insulating layer", as recited in Claim 17. Kenney also does not describe or suggest that the read only memory programming region is an implant region, as recited in Claim 18.

Applicants also wish to note that Claims 17 and 18 were rejected in the second paragraph of Page 3 of the Official Action based on Kenney allegedly disclosing a programming region at Column 5, lines 44-48. However, the portion of Kenney that includes this passage clearly states:

> Depending upon the material and thickness of gate electrode layer **24**, photoresist plug **28** may or may not be retained to act as a further mask to the implanted ions over the channel region of the device. Shading lines in FIG. 9 show the areas of the substrate which are implanted. Ion implanted regions **30** act as source/drain regions of the MOSFET device being formed and also provide low resistance interconnection between adjacent devices in the array.

This passage clearly relates to implanting of source and drain regions, and does not relate to a programming region as recited in Claims 17 and 18. This lack of disclosure is consistent with the fact that Kenney relates to a dynamic random access memory that includes a single FET/capacitor memory cell, and does not relate to a read only memory. Accordingly, Claims 17 and 18 are independently patentable.

New Claims 20-24 Are Patentable

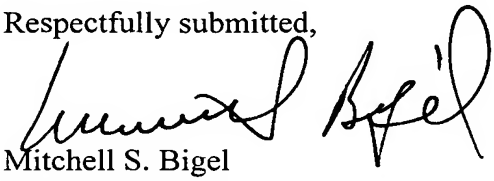
Claim 20 includes the recitations of Claim 14 as filed, and also incorporates therein the recitations of Claim 17. As was already described above in connection with Claim 17, Kenney does not describe or suggest a ROM programming region in

the integrated circuit substrate beneath the insulating layer, because Kenney does not relate to read only memory devices, but, rather, relates to dynamic random access memory devices. Accordingly, Claim 20 is patentable over Kenney. Claims 21-24 are patentable at least per the patentability of Claim 20 from which they depend.

Conclusion

Applicants again appreciate the thorough examination and the citation of Kenney. The claims have now been amended and new claims have been added to clarify the patentable distinctions over Kenney. Accordingly, Applicants respectfully request allowance of the present application and passing the application to issue.

Respectfully submitted,



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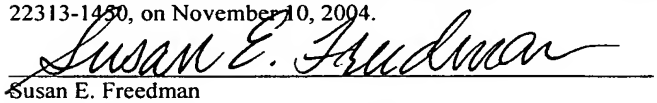

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Date of Signature: November 10, 2004